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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Papers

Application of:

Applicant : Nicholas Paul Cowley et al.
Serial No. : 10/004,766
Filed : 12/04/2001
Title : RADIO FREQUENCY TUNER
Docket No. : 534334-020

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Assistant Commissioner for Patents
Washington, D.C. 20231

SUBMISSION OF PRIORITY DOCUMENTS

Pursuant to the claim for priority under 35 U.S.C. §119 made in the Declaration in the above-identified application, the following priority document is submitted:

<u>Country</u>	<u>Application No.</u>	<u>Filing Date</u>
Great Britain	0029564.2	December 5, 2000
Great Britain	0110607.9	May 1, 2001

No fee is required. The Commissioner is authorized to charge any additional fees required by this paper (including the fee for any additional extension of time) or to credit any overpayment to Deposit Account No. 20-0809.

Respectfully submitted:

Date: February 21, 2002

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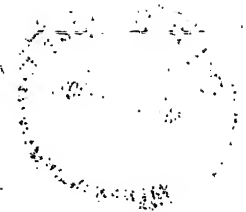
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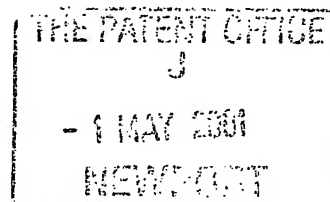
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Cardiff Road
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1. Your reference JSR.P51556GB

2. Patent application number
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0110607.9

01 MAY 2001

3. Full name, address and postcode of the or of each applicant (underline all surnames)

Mitel Semiconductor Limited
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Patents ADP number (if you know it) 73 8744 2001

If the applicant is a corporate body, give the country/state of its incorporation AB UK
ATL 15/6/01

4. Title of the invention Radio Frequency Tuner

5. Name of your agent (if you have one)

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"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

4220 Nash Court
Oxford Business Park South
Oxford OX4 2RU
United Kingdom

7271125001 ✓

Patents ADP number (if you know it)

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Country

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Priority documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (Patents Form 7/77)

Request for preliminary examination and search (Patents Form 9/77)

1

Request for substantive examination (Patents Form 10/77)

Any other documents
(please specify)

11.

I/We request the grant of a patent on the basis of this application.

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Date

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30 April 2001

12. Name and daytime telephone number of person to contact in the United Kingdom. John S. Robinson - 01865 397900

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1. Your reference JSR.P51556GB
2. Patent application number
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3. Full name of the or of each applicant Mitel Semiconductor Limited

4. Title of the invention
Radio Frequency Tuner

5. State how the applicant(s) derived the right
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Marks & Clerk 14 May 2001

8. Name and daytime telephone number of
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51122-8B-37

Patents Form 7/77

Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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Radio Frequency Tuner

The present invention relates to a radio frequency tuner. Such a tuner may be used as a cable tuner for receiving modulated digital signals from a cable distribution network, for example, as a set top box for receiving television signals. Other applications include use for cable telephony and as a modem for data signals.

Known types of cable tuners may be of the single conversion or double conversion type. By way of illustration, Figure 1 of the accompanying drawings illustrates a double conversion cable tuner for digital signals. The tuner has an input 1 for connection to a cable distribution network and connected to an automatic gain control (AGC) stage 2. The output of the stage 2 is connected to a first frequency changer 3 for performing up-conversion and comprising a mixer 4 and a local oscillator 5 controlled by a phase locked loop (PLL) synthesiser 6.

The output of the first frequency changer 3 is connected via a first intermediate frequency filter 7 to a second frequency changer 8 of the down-conversion type. The second frequency changer 8 comprises a mixer 9 and a local oscillator 10 controlled by a PLL synthesiser 11. The output of the second frequency changer 8 is supplied by a second intermediate frequency filter 12 to an intermediate frequency (IF) amplifier 13 whose output supplies an IF signal to the output 14 of the tuner.

Figure 2 of the accompanying drawings illustrates a typical cable distribution system. The system comprises an optical fibre "backbone" 20 which supplies a plurality of head end distribution units 21. Each of the units 21 services a plurality of properties, such as houses and offices, as illustrated at 22. A cable 23 connects each property to its head end unit 21, which supplies the signals from the distribution network and which also supplies power to a modem 24 including a tuner of the type shown in Figure 1. The modem 24 is continuously powered and supplies a telephony service by means of a conventional twisted pair 25 and a cable service for further modem applications such as television and internet as illustrated at 26.

The tuner is required to convert any selected channel from the cable distribution network to an intermediate frequency in the form of a signal having characteristics which are sufficient to ensure acceptable perceived performance. For example, the signal to noise plus intermodulation performance must be sufficient for acceptable television or data signals to be provided. The signals from the cable distribution network are supplied to the AGC stage 2 which controls the signal level supplied to the first frequency changer 3 so as to provide an acceptable intermodulation performance of the first frequency changer. In general, little or no filtering takes place before the frequency changer 3, which is therefore required to have a high level of performance.

The frequency changer 3 performs block up-conversion of the broad band input signal with the frequency of the local oscillator 5 being selected by the synthesiser 6 such that a desired channel is centred on a high first intermediate frequency. The synthesiser 6 and the synthesiser 11 are, for example, controlled via an I2C bus micro-controller (not shown).

The output of the first frequency changer 3 is filtered by the filter 7, which has a centre frequency at the predetermined first intermediate frequency and a pass-band characteristic such that the desired channel and a small number of further channels on either side of the desired channel are supplied to the second frequency changer 8.

The second frequency changer 8 performs a block down-conversion such that the desired channel is centred on the second much lower intermediate frequency. The output signal of the second frequency changer 8 is filtered by the filter 12 whose centre frequency is centred on the centre frequency of the desired channel following the second conversion and which has a pass-band for passing the desired channel and for rejecting or substantially attenuating the adjacent channels. The desired channel at the second intermediate frequency is amplified by the amplifier 13 and supplied to the tuner output 14.

Known types of tuner (of the type shown in Figure 1 and of other types such as the single conversion type) are required to be able to cope with all extremes of signal

conditions. In particular, such tuners are required to handle a wide dynamic range of signals and to cope with worst case composite signal loading, maximum channel to channel ripple and various other conditions, both singly and in any combination.

As a result of these requirements, for much of the time during operation, each tuner in a cable distribution system provides a much higher performance than is actually required by the individual channels being received. For example, in the case of modulated digital signals, there is no advantage in providing a tuner performance which exceeds a threshold value for signal to noise plus intermodulation performance. In such cases, the presence of complex Forward Error Correction techniques, such as Reed Solomon Coding and Viterbi-puncturing, means that there is no or no perceivable improvement in reception when a minimum threshold of signal to noise plus intermodulation is achieved.

The power consumption of a tuner is generally a direct function of the performance of the tuner. The term "direct function" in this context means that, for over at least a range of power consumptions, the performance of the tuner is a monotonic function of the power consumption of the tuner. Thus, more power is consumed, for example from the cable distribution network powering the modems²⁴, than is necessary to achieve the desired performance. Unnecessary power consumption is undesirable for many reasons, such as cost and environmental factors. With the increasing use of cable distribution systems and consequently of modems incorporating such tuners, the problem of increased power consumption is in turn increasing and is undesirable.

Known types of tuners, such as that illustrated in Figure 1, are individually designed for different applications. For example, the reception of analogue signals requires very low intermodulation and cross-modulation generation but the phase noise requirement is not particularly demanding. On the other hand, reception of digital signals does not require such low intermodulation and cross-modulation generation but a better phase noise performance is required. Thus, individual tuners are specifically designed for different applications and this particularly affects the frequency changers. In particular, such tuners are designed in accordance with the modulation standard which they are required

to receive. It has therefore not been possible to provide a "universal" tuner design which can be used for many different applications because achievement of the specification required to meet all standards would result in a non-optimum design having high power consumption and being commercially unattractive or unacceptable.

According to the invention, there is provided a radio frequency tuner comprising at least one stage whose performance is a function of power consumption thereof and a power consumption control circuit for controlling the power consumption of the at least one stage.

The control circuit may be responsive to means for setting the power consumption to achieve a desired tuner performance.

The performance of the at least one stage may be a direct function of the power consumption thereof.

The setting means may comprise a comparator for comparing the tuner performance with a first predetermined performance and for causing the control circuit to reduce the power consumption of the at least one stage when the tuner performance exceeds the first predetermined performance.

The comparator may be arranged to compare the tuner performance with a second predetermined performance lower than the first predetermined performance and the control circuit may be arranged to increase the power consumption of the at least one stage when the tuner performance is less than the second predetermined performance.

The tuner performance may be the ratio of signal to noise plus intermodulation products.

The tuner may comprise a digital tuner. The tuner may comprise a demodulator and the tuner performance may be the bit error rate.

The first predetermined performance may be greater than an acceptable minimum performance. The second predetermined performance may be less than or equal to the acceptable minimum performance.

The bit error rate may be the instantaneous bit error rate, a time-averaged bit error rate, or a combination thereof.

The comparator may be arranged to perform the comparison continuously. As an alternative, the comparator may be arranged to perform the comparison periodically. As another alternative, the comparator may be arranged to perform the comparison each time the tuner is powered up. As a further alternative, the comparator may be arranged to perform the comparison each time a change of tuned frequency is requested.

The setting means may comprise means for selecting a desired power consumption. The selecting means may be arranged to select the desired power consumption from a plurality of fixed power consumptions.

The setting means may comprise a control input of the control circuit.

The setting means may be arranged to fix the power consumption during manufacture of the tuner.

The at least one stage may comprise at least one frequency changer stage. The at least one frequency changer stage may comprise at least one mixer whose transconductance is dependent on power consumption. The at least one mixer may comprise at least one load whose value is adjustable to compensate for changes in the transconductance. The at least one mixer may comprise an image reject mixer. The at least one frequency changer stage may comprise at least one low noise amplifier whose gain is dependent on power consumption. The at least one frequency changer stage may comprise at least one local oscillator whose power consumption is controllable by the control circuit.

The at least one stage may comprise at least one intermediate frequency amplifier. The at least one intermediate frequency amplifier may have a gain which is controllable by the control circuit.

The tuner may comprise a cable tuner.

The tuner may be formed as a single monolithic integrated circuit.

It is thus possible to provide a tuner whose power consumption can be selected according to the performance which is required of the tuner. For any particular application of the tuner, the power consumption can be reduced, minimised or optimised. This may be achieved automatically or manually.

For example, the power consumption may be controlled automatically so as to provide a tuner of reduced power consumption compared with known types of tuner. The tuner can ensure, particularly but not exclusively in the case of a digital tuner for receiving digitally modulated signals, that an acceptable performance is provided for the signal or channel currently being received while reducing or minimising the power consumption. Although such a tuner may be used for any application, it may be used with advantage in cable distribution systems of the type described hereinbefore. Where such tuners are powered by the cable distribution system, the power consumption of the system can be reduced or minimised to provide a substantially lower power consumption than the known type of system. This can be achieved without any or any perceptible degradation in the received signals.

In another example, the power consumption may be set in a way which does not depend on the reception performance actually achieved by the tuner. The power consumption may be set during or after manufacture and this allows a single design of tuner to be adapted easily for any of a plurality of different applications. For example, such a tuner may be set to have: a relatively high power consumption so as to provide good intermodulation performance for analogue reception; a range of reduced power consumptions for various digital applications having various intermodulation

performance requirements; a low power consumption for use in cable powered equipment.

Digital applications require the local oscillator of a frequency changer to have low phase noise, and hence relatively high power consumption, whereas analogue applications are less sensitive to phase noise. Local oscillator power consumption can thus be set according to the tuner application so as to allow tuner power consumption to be substantially optimised for each application.

It is thus possible to provide a "universal" tuner which is suitable for different applications. Design time and cost and manufacturing cost may therefore be reduced.

The present invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block circuit diagram of a known type of double conversion cable tuner;

Figure 2 is a block schematic diagram of a known type of cable distribution system;

Figure 3 is a block circuit diagram of a cable tuner constituting an embodiment of the invention;

Figure 4 is a block circuit diagram showing in more detail one of the stages of the tuner shown in Figure 3; and

Figure 5 is a block circuit diagram of a cable tuner constituting another embodiment of the invention.

Like reference numerals refer to like parts throughout the drawings.

The digital cable tuner shown in Figure 3 is of the double-conversion type and is similar to that illustrated in Figure 1. Accordingly, only the aspects of construction and

operation which differ from those described with reference to Figure 1 will be described in detail.

The output of the IF amplifier 13 is connected to a demodulator 30 for demodulating the selected received channel in accordance with the type of modulation which it uses. For example, the demodulator 30 may be arranged to demodulate quadrature amplitude modulated signals in order to extract the required digital data, for example for television reception.

The demodulator 30 comprises an analogue/digital converter (ADC) stage 31 which converts the incoming IF signal to a corresponding digital signal. A forward error correction (FEC) stage 32 performs error correction and the corrected signal is supplied to a demodulator stage 33 which supplies the output signal of the demodulator 30. The demodulator 30 also comprises a bit error rate (BER) estimator 34, which provides a signal representing the bit error rate. This rate may be the instantaneous rate, a time averaged value, or any appropriate indication of the bit error rate suitable for the subsequent processing as described hereinafter.

The tuner comprises a microcontroller 35 which is connected to various parts of the tuner by means of a I2C bus 36. The microcontroller 35 sends and receives data via the bus 36 and performs various control operations, for example including controlling the synthesisers 6 and 11 so as to ensure that a channel selected for reception is correctly tuned. The microcontroller 35 receives data from the demodulator 30 including the bit error rate value provided by the estimator 34. In addition to the synthesisers 6 and 11, the microcontroller 35 controls the power consumption of the frequency changers 3 and 8 and the IF amplifier 13 via the bus 36.

The frequency changers 3 and 8 are modified as compared with the corresponding frequency changers shown in Figure 1 as illustrated in Figure 4. Thus, each frequency changer has a radio frequency (RF) input connected to a mixer stage 40 comprising a low noise amplifier (LNA) 41 and a mixer 4, 9. The local oscillator 5, 10 comprises a voltage controlled oscillator (VCO) whose output is connected to a signal splitter 42,

which supplies the local oscillator signal to the mixer 4, 9 and to the frequency synthesiser 6, 11. The frequency changer comprises a bus interface 43 having an input 44 for connection to the bus 36 and output busses connected to the frequency synthesiser 6, 11, the mixer stage 40 and an IF amplifier 45 whose input is connected to the output of the mixer 4, 9 and whose output 46 constitutes the IF output of the frequency changer.

The frequency synthesiser 6, 11 is controlled in the conventional way via the bus interface 43 so that the VCO 5, 10 is tuned to the desired frequency for converting the selected channel to the desired output intermediate frequency. The mixer stage 40 has a control input connected to the interface 43 so as to control the power consumption of this stage. Thus, the microcontroller 35 can control the power consumption of the mixer stage 40 via the bus 36, the input 44, and the bus interface 43. The power consumption of the LNA 41 or of the mixer 4, 9 or of both of these may be controlled.

The performance of the mixer stage 40 depends on its power consumption. In particular, the transconductance g_m and hence the gain is a direct function of the power consumption of this stage. Further, the intermodulation performance is a direct function of the power consumption. Thus, throughout at least a part of the range of power consumptions of this stage, as the power consumption is increased, the transconductance, gain and the intermodulation performance all increase or improve monotonically.

In order to compensate for variations in gain as a result of variations in transconductance resulting from varying the power consumption of the stage 40, the LNA 41 or the mixer 4, 9 or both may have a load whose value is varied simultaneously with varying the power consumption of the stage. Such an arrangement allows changes in gain resulting from changing the power consumption of this stage to be at least partly compensated. However, although it is possible to compensate for gain variations as a result of controlling the power consumption, other aspects of performance such as the intermodulation performance are reduced as the power consumption of the stage is reduced.

The bus interface 43 is also connected to the IF amplifier or buffer 45 in order to control its power consumption. Again, as the power consumption of the buffer 45 is reduced, its transconductance and hence its gain is reduced. Again, the buffer 45 may have a programmable load impedance which is controlled so as to compensate at least partly for reduced transconductance with power consumption in order to restore at least partly the gain of this stage and make it less sensitive to changes in power consumption.

The interface 43 is also connected to the VCO 5, 10 so as to control the power consumption of the oscillator. As the power consumption is reduced, the phase noise performance of the oscillator 5 is reduced.

When the tuner shown in Figures 3 and 4 is initially powered and/or periodically thereafter, an adjustment routine is controlled by the microcontroller 35 in order to minimise the tuner power consumption while maintaining an acceptable minimum performance for reception of a selected desired channel. Initially, the power consumption of the tuner, particularly the frequency changers 3 and 8 and the IF amplifier 13, is set to a maximum value so that the tuner operates at its best performance level, for example in terms of signal to noise plus intermodulation performance. The microcontroller 35 controls the synthesisers 6 and 11 in accordance with a user request to select and receive a desired channel from the range of channels supplied to the tuner via the cable distribution network. The AGC stage 2, the frequency converters 3 and 8, the filters 7 and 12 and the amplifier 13 perform as described hereinbefore with reference to Figure 1.

The demodulator 30 digitises and error-corrects the IF signal, which is then demodulated to supply the channel signal, for example to a television receiver in the case of a channel providing a television service. The estimator 34 estimates the bit error rate and supplies this to the microcontroller 35. The demodulator 30 also supplies to the microcontroller 35 data indicating the type of modulation scheme used by the selected channel. For example, in the case of quadrature amplitude modulation (QAM), the demodulator indicates to the microcontroller 35 which QAM level is employed by the selected channel.

The microcontroller 35 determines on the basis of the type of modulation scheme and, in particular, the QAM level an acceptable performance for the selected channel. In the case of QAM, a high level modulation scheme such as "QAM 256" requires a higher level of tuner performance than a lower level modulation scheme, such as "QAM 16". The microcontroller 35 derives from the acceptable performance first and second predetermined performances which are higher and lower than the acceptable performance and compares the bit error rate from the estimator 34 with the first and second predetermined performances. If the bit error rate is such that the tuner performance exceeds the first pre-determined performance, the microcontroller 35 reduces the power consumption of the first frequency changer 3 by supplying the appropriate control signal as data via the bus 36, the input 44 and the bus interface 43 of the first frequency changer. In particular, the power consumption of the mixer stage 40 is reduced and this reduces the performance, particularly the signal to noise plus intermodulation performance, of the first frequency changer 4.

For as long as the bit error rate indicates a tuner performance in excess of the first predetermined performance, the power consumption of the first frequency changer 3 is incrementally reduced and this process stops when the performance falls below the first predetermined performance. If the minimum power consumption of the first frequency converter 3 is reached before the performance falls below the first predetermined performance, then the power consumption of the second frequency changer 8 is incrementally reduced until it reaches a minimum permitted power consumption or its performance falls below the first determined performance. Thus, in this example, the full power consumption range of the first converter 3 is used before adjusting the power consumption of the second frequency converter. However, other control algorithms are possible and, for example, the microcontroller 35 may increment the power consumptions of the first and second frequency changers alternately. Also, the power consumptions and hence performances of other stages, such as the oscillators 5 and 10, the buffers 45 and the amplifier 13 may be controlled using any appropriate strategy.

If the performance of the tuner as indicated by the bit error rate falls below the second predetermined performance, then the control algorithm is reversed and the power

consumption is increased. In the previously described case where the full power consumption range of the first frequency changer 3 is used before adjusting the power consumption of the second frequency changer 8, the power consumption of the second frequency changer 8 is incremented upwardly to its maximum value and this is then repeated for the first frequency changer 3 until the performance exceeds the second predetermined performance. The gap between the first and second predetermined performances provides hysteresis to ensure stable operation of the control algorithm. Although the second predetermined performance has been indicated as being below the acceptable performance, it is also possible for the second predetermined performance to be equal to or greater than the acceptable performance but it should always be less than the first pre-determined performance.

This control algorithm may be performed on initially powering the tuner with the performance then remaining fixed until the tuner is depowered and repowered. As an alternative, the algorithm may be performed periodically whenever the tuner is powered. As a further alternative, this algorithm may be performed only when a different channel is selected by a user so as to ensure that the tuner power consumption is minimised for the selected channel while ensuring that the selected channel is received with acceptable performance.

The increments in power consumption of the or each controlled stage may be chosen so as to provide a desired overall performance of the tuner. For example, fixed increments may be used, in which case the degree of power consumption minimisation depends on the increment size, as does the rate at which the power consumption converges to a steady or more steady state. Alternatively, the increment sizes may be a function of the difference between the current tuner performance and the acceptable performance. Such an arrangement provides a more rapid convergence but requires a slightly more complex control algorithm.

It is thus possible to minimise or at least reduce the power consumption of the tuner while maintaining acceptable performance for the received signals. In the case of digitally encoded signals, once an acceptable performance has been achieved, there is

no need for a better tuner performance, which would require greater power consumption. The tuner may therefore be operated such that its power consumption is substantially less than would have to be provided by a known type of tuner without any perceivable degradation in the received signals.

The tuner shown in Figure 5 differs from that shown in Figure 3 in various ways and allows the power consumption and hence the performance of the tuner to be set independently of the actual performance being achieved by the tuner. Thus, the demodulator 30 is not necessary to the functioning of the tuner of Figure 5, and has been omitted from the drawing. The microcontroller 35 does not perform the adjustment routine described hereinbefore but instead has an input 38 which allows the power consumption and hence performance of each of the stages whose power consumption can be controlled to be adjusted or selected independently of the other stages. The input 38 to the microcontroller 35 is shown by way of example only and any other control input arrangement or power consumption setting arrangement which allows the individual stage power consumptions to be selected may be used.

The power consumption of each stage may be selected continuously or may be selected from a plurality of pre-set available power consumptions. The power consumptions may be set during manufacture of the tuner so as to adapt it to a specific application or may be made available to a user to select the stage power consumptions in order to adapt a standard or "universal" tuner design to a specific application.

The frequency changers 3 and 8 of Figure 5 are of the same type as shown in Figure 4. Although the mixer stage 40 is shown as having a separate low noise amplifier 41 from the mixer 4, 9, the low noise amplifier and mixer may be combined as a single stage with the input transconductance of the mixer forming the low noise amplifier.

The standing or quiescent current of either or both of the low noise amplifier and the mixer 4, 9 can be adjusted by the microcontroller 35 via the bus 36, the input 44 and the interface 43 in accordance with a preset desired standing current set via the input 38.

Adjusting the standing current, and hence the power consumption, of the mixer stage 40

allows the transconductance of the stage to be adjusted. As the standing current is reduced, the power consumption of the frequency changer is reduced and the noise figure is improved. The resulting improvement in the noise figure allows the frequency changer to be operated at a lower input signal level while maintaining the same signal-to-noise ratio. A consequence of this is that the intermodulation performance improves. Reducing the standing current allows the second order intermodulation performance to be substantially maintained but the third order intermodulation performance is reduced. The gain of the stage is reduced but this may be compensated if necessary, for instance by providing a programmable load at the output of the mixer stage so as to maintain the gain or by providing the facility of an externally mounted component which may be selected so as to maintain the gain.

The same mechanism is used to control the power consumption and hence the phase noise performance of the local oscillators 5 and 10 in accordance with a selection signal at the input 38. This allows the same tuner design to be used for a variety of applications and permits the power consumption of the tuner to be optimised for each application. For example, if the tuner is required to receive analogue signals, the standing currents and hence the power consumptions of the mixer stages 40 are set to high values so as to provide the necessary intermodulation and cross-modulation distortion performance. However, because phase noise performance does not have to be particularly good for analogue signals, the power consumptions of the local oscillators 5, 10 may be reduced. For reception of digital signals where the intermodulation and cross-modulation performances are less critical but a high phase noise performance is required, the power consumptions of the mixer stages 40 can be selected at a lower level and the power consumptions of the oscillators 5, 10 at a higher level in accordance with the particular digital modulation standard being used. For applications where the tuner is powered from the cable distribution network, the various stage power consumptions can be set to the minimum value consistent with obtaining adequate performance for the signals being received.

CLAIMS:

1. A radio frequency tuner comprising at least one stage whose performance is a function of power consumption thereof and a power consumption control circuit for controlling the power consumption of the at least one stage.
2. A tuner as claimed in claim 1, in which the control circuit is responsive to means for setting the power consumption to achieve a desired tuner performance.
3. A tuner as claimed in claim 2, in which the performance of the at least one stage is a direct function of the power consumption thereof.
4. A tuner as claimed in claim 3, in which the setting means comprises a comparator for comparing the tuner performance with a first predetermined performance and for causing the control circuit to reduce the power consumption of the at least one stage when the tuner performance exceeds the first predetermined performance.
5. A tuner as claimed in claim 4, in which the comparator is arranged to compare the tuner performance with a second predetermined performance lower than the first predetermined performance and the control circuit is arranged to increase the power consumption of the at least one stage when the tuner performance is less than the second predetermined performance.
6. A tuner as claimed in claim 4 or 5, in which the tuner performance is the ratio of signal to noise plus intermodulation products.
7. A tuner as claimed in any one of claims 4 to 6, comprising a digital tuner.
8. A tuner as claimed in claim 7, in which the tuner comprises a demodulator and the tuner performance is the bit error rate.

9. A tuner as claimed in any one of claims 4 to 8, in which the first predetermined performance is greater than or equal to an acceptable minimum performance.
10. A tuner as claimed in claim 9 when dependant on claim 5, in which the second predetermined performance is less than or equal to the acceptable minimum performance.
11. A tuner is claimed in claim 8 or in claim 9 or 10 when dependant on claim 8, in which the bit error rate is the instantaneous bit error rate.
12. A tuner as claimed in claim 8 or in claim 9 or 10 when dependant on claim 8, in which the bit error rate is a time-averaged bit error rate.
13. A tuner as claimed in Claim 8 or in claim 9 or 10 when dependent on claim 8, in which the bit error rate is a combination of the instantaneous bit error rate and a time-averaged bit error rate.
14. A tuner as claimed in any one of claims 4 to 13, in which the comparator is arranged to perform the comparison continuously.
15. A tuner as claimed in any one of claims 4 to 13, in which the comparator is arranged to perform the comparison periodically.
16. A tuner as claimed in any one of claims 4 to 13, in which the comparator is arranged to perform the comparison each time the tuner is powered up.
17. A tuner as claimed in any one of claims 4 to 13, in which the comparator is arranged to perform the comparison each time a change of tuned frequency is requested.
18. A tuner as claimed in claim 2 or 3, in which the setting means comprises means for selecting a desired power consumption.

19. A tuner as claimed in claim 18, in which the selecting means is arranged to select the desired power consumption from a plurality of fixed power consumptions.

20. A tuner as claimed in claim 2 or 3, in which the setting means comprises a control input of the control circuit.

21. A tuner as claimed in claim 2 or 3, in which the setting means is arranged to fix the power consumption during manufacture of the tuner.

22. A tuner as claimed in any one of the preceding claims, in which the at least one stage comprises at least one frequency changer stage.

23. A tuner as claimed in claim 22, in which the at least one frequency changer stage comprises at least one mixer whose transconductance is dependant on power consumption.

24. A tuner as claimed in claim 23, in which the at least one mixer comprises at least one load whose value is adjustable to compensate for changes in the transconductance.

25. A tuner as claimed in claim 23 or 24, in which the at least one mixer comprises an image reject mixer.

26. A tuner as claimed in any one of claims 22 to 25, in which the at least one frequency changer stage comprises at least one low noise amplifier whose gain is dependent on power consumption.

27. A tuner as claimed in any one of claims 22 to 26, in which the at least one frequency changer stage comprises at least one local oscillator whose power consumption is controllable by the control circuit.

28. A tuner as claimed in any one of the preceding claims, in which the at least one stage comprises at least one intermediate frequency amplifier.

29. A tuner as claimed in claim 28; in which the at least one intermediate frequency amplifier has a gain which is controllable by the control circuit.

30. A tuner as claimed in any one of the preceding claims, comprising a cable tuner.

31. A tuner as claimed in any one of the preceding claims, formed as a single monolithic integrated circuit.

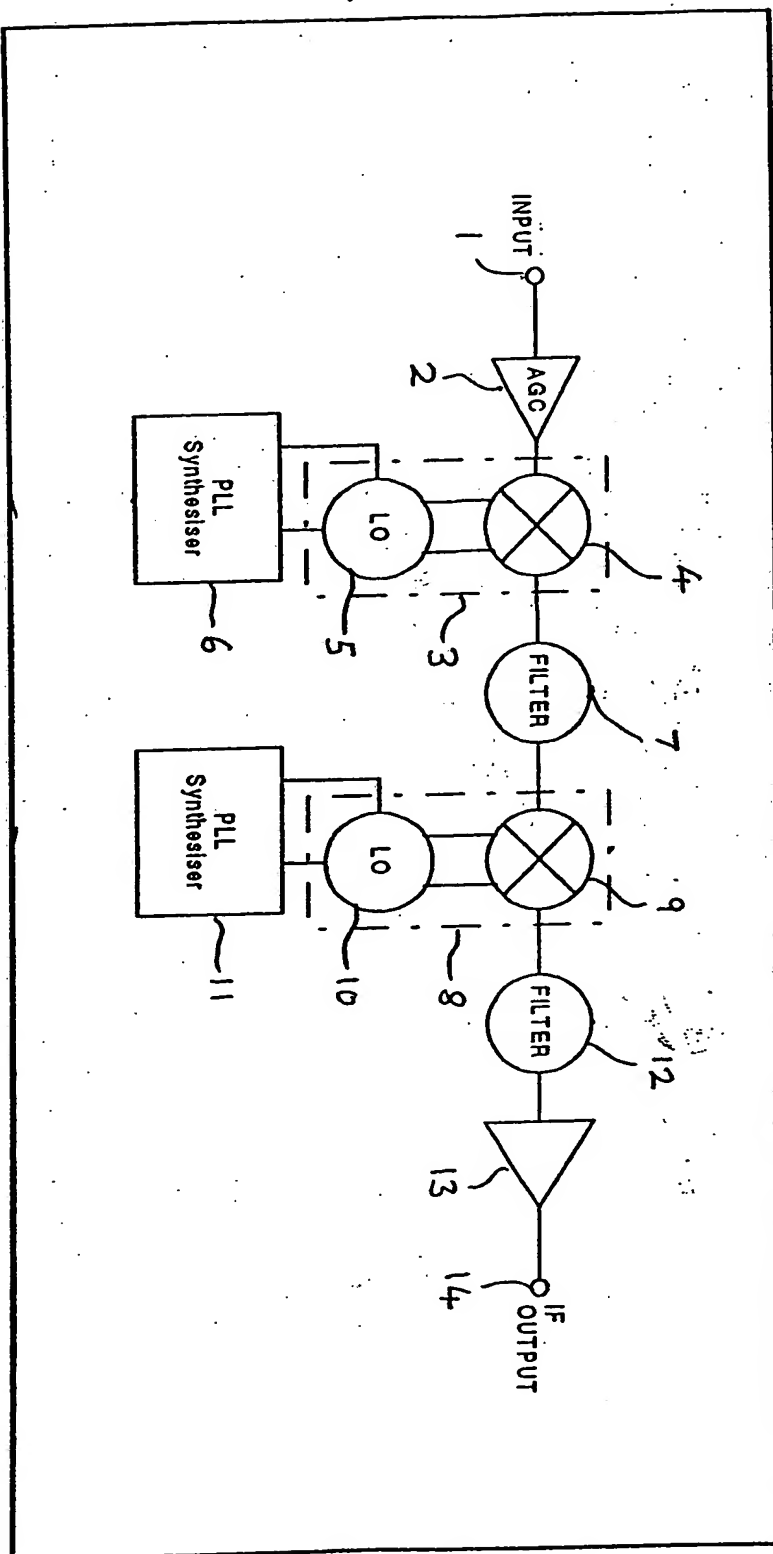
ABSTRACT**Radio Frequency Tuner .**

A radio frequency tuner is provided for selecting channels from a cable distribution network or other reception system. The tuner has one or more stages (3, 8, 13) whose performance, such as signal to noise plus intermodulation, is a function of the stage power consumption. A comparator (35) compares the tuner performance, such as bit error rate (34), with a predetermined performance. When the tuner performance exceeds the predetermined performance, a power consumption control circuit (35) reduces the power consumption of one or more of the stages (3, 8, 13) so as to reduce the tuner power consumption while maintaining acceptable tuner performance. As an alternative, the control circuit (35) may have an input (38) which allows the power consumption to be preset in accordance with the tuner application.

(Figure 3)

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Fig 1



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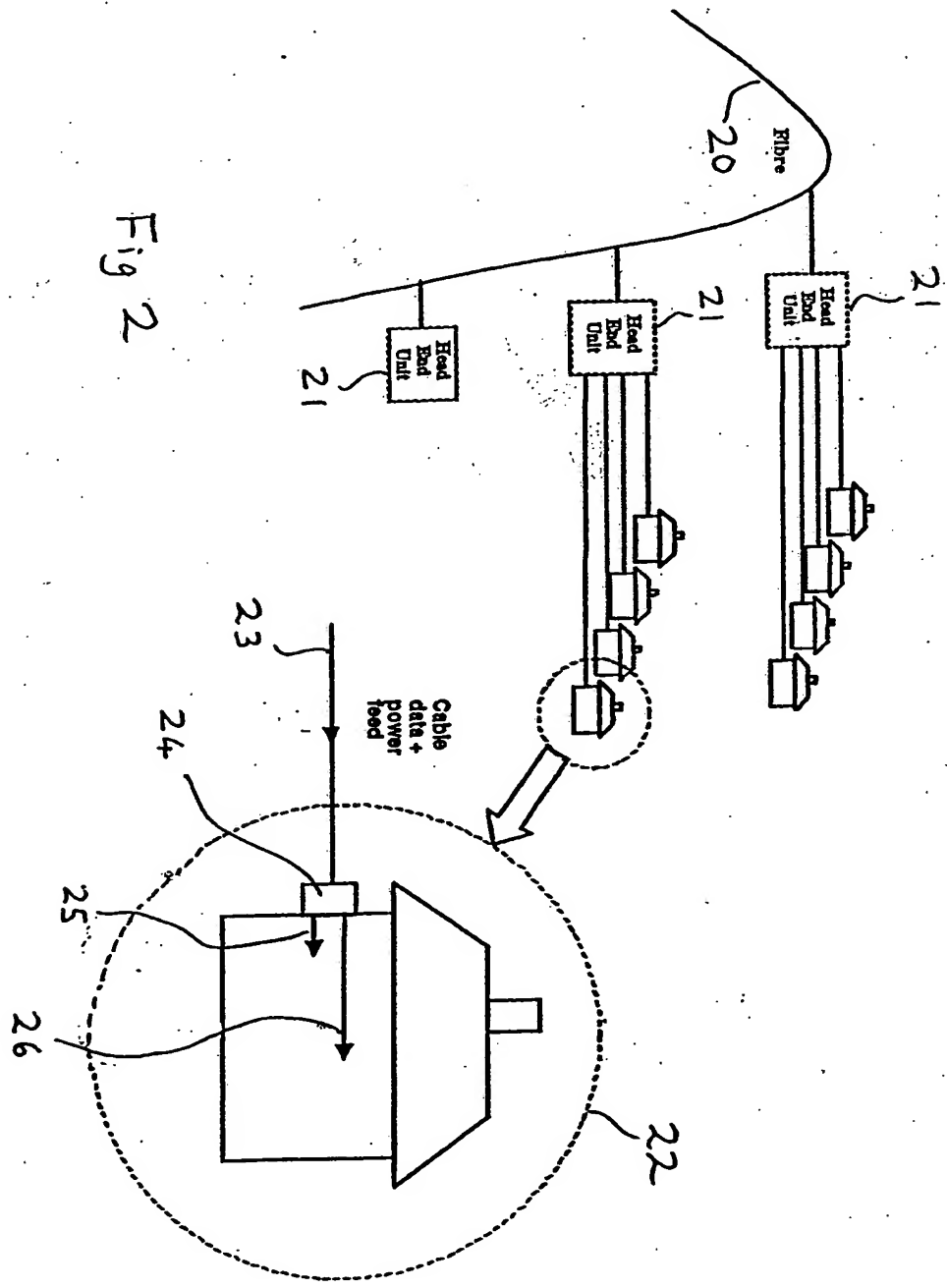


Fig 2

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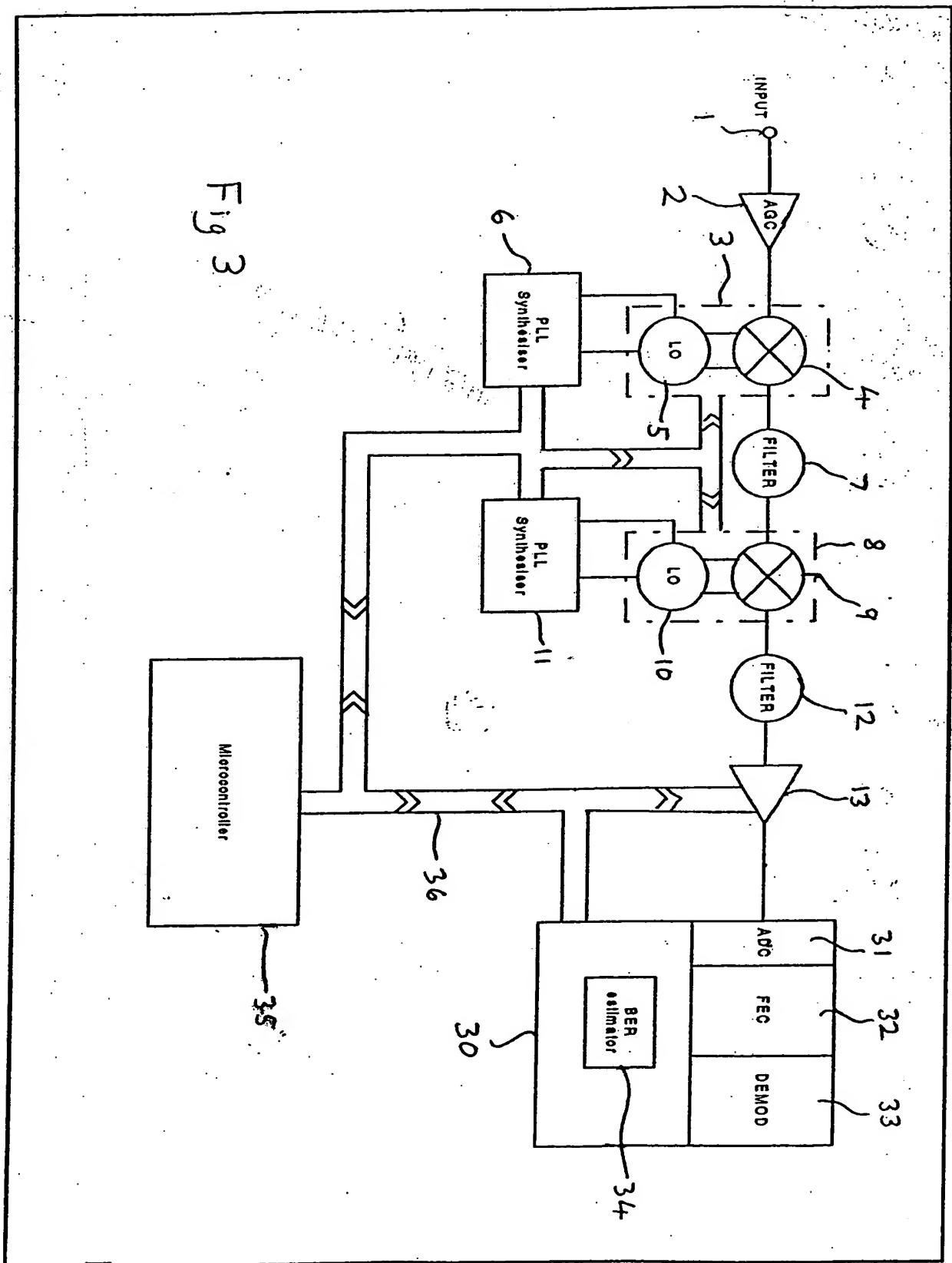
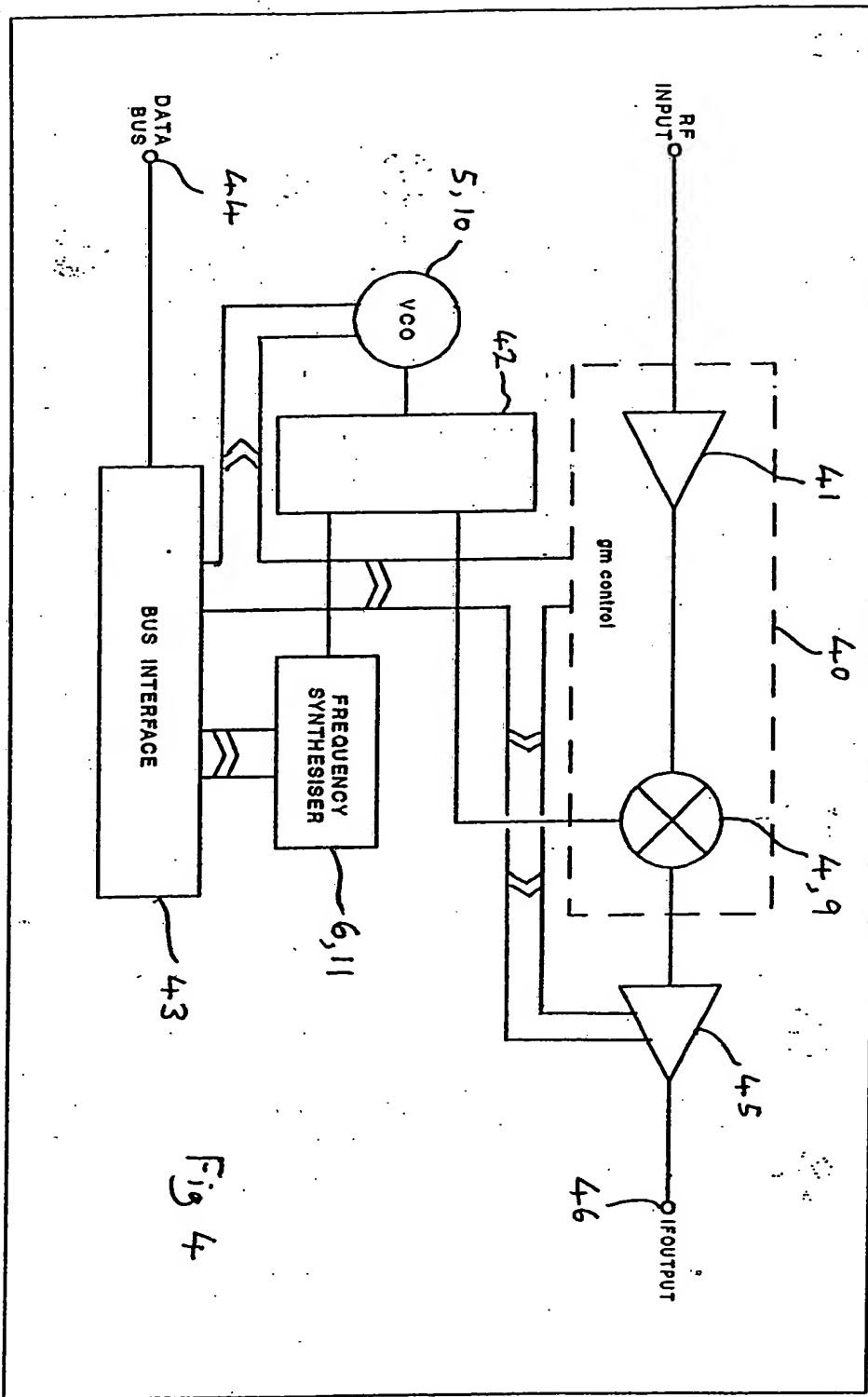


Fig 3

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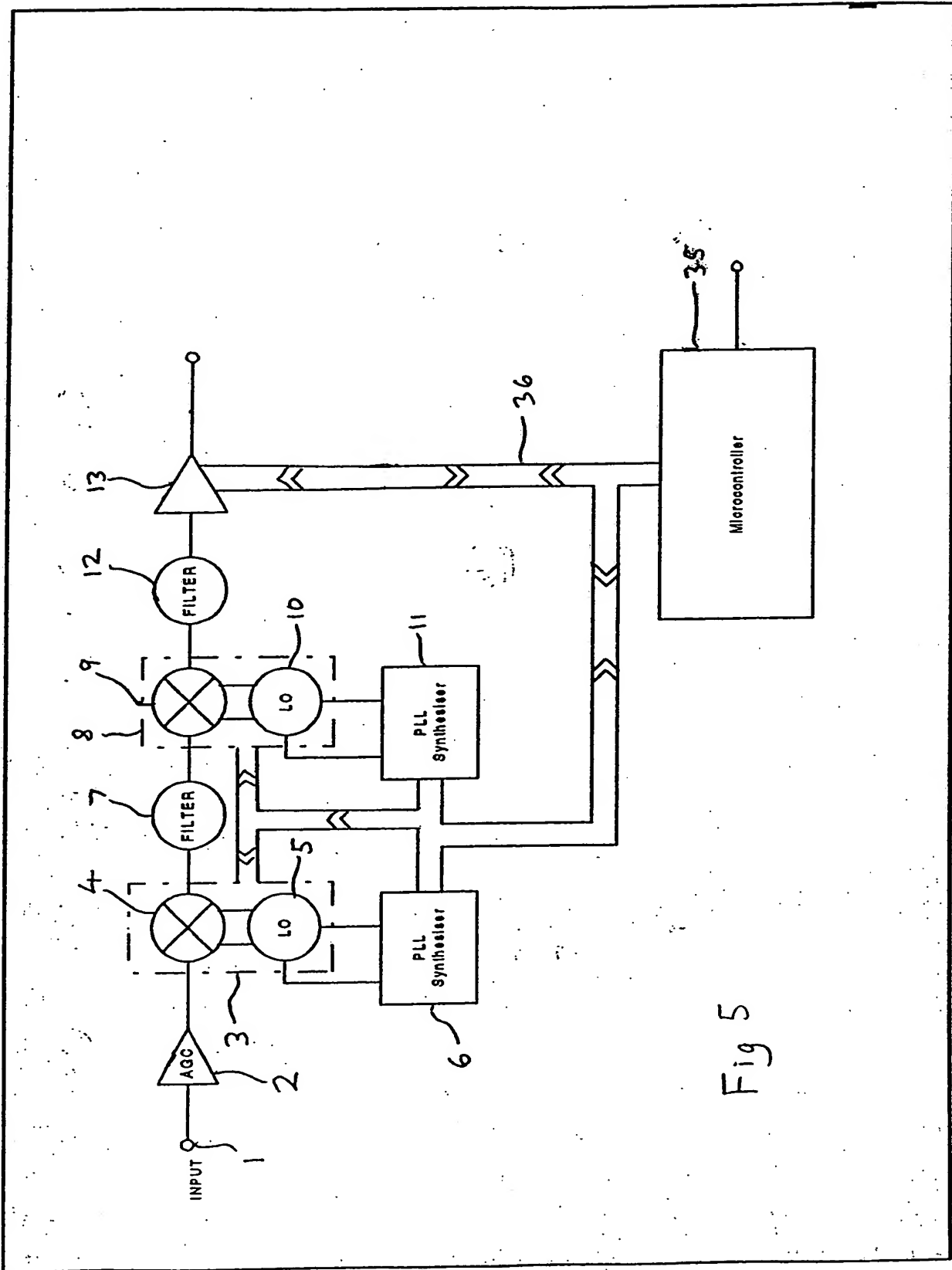


Fig 5

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